

NCS Standard Computer Interface Hardware, Its Timing and Timing Control Logic

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This article describes the Network Control System (NCS) Standard Computer Interface hardware, including the interface cable, the line drivers, line receivers and line terminating network. It describes in considerable detail the timing specifications for the interface timing control signals for continuous data transfer as well as for asynchronous byte transfer. A set of control logic which complies with these timing specifications has been designed for and successfully checked out in connection with the Star Switch Controller (SSC). This control logic, which includes synchronization and noise filter operations, is described in detail. Transfer rates for variable cable lengths are listed.

I. Introduction

The NCS standard computer interface hardware contains 14 parallel data-transmission lines. Eight of these lines are data lines, four are timing and control lines, and two are function lines (see Fig. 1).

Of the interface timing control lines for asynchronous data transmission, two are unidirectional request lines, one in each direction; one is a bidirectional half-duplex response line; and one is a bidirectional half-duplex ready line. The linear bit operation of these lines and the operation of the control logic to perform these operations is specified in detail. The control logic synchronizes the input signals to the local service clocks, and filters out spurious noise pulses of short duration. Both the control

logic and its operation are described in detail, as are the cable, line drivers, receivers, and line termination.

II. Cable, Drivers, Receivers, and Line Termination

The NCS standard interface cable is a twisted pair cable, with line drivers and line receivers, as shown in Figs. 2 and 3. The cable itself is shown in Fig. 4. All connectors, physically and functionally, mate with connectors such as that shown in Fig. 4. Pin assignments for the timing control lines, data lines, and function lines are also shown in Fig. 4. (Figures 2, 3, and 4 are taken from JPL Specification ES508534 A, May 1973, a JPL internal document.)

As shown in the figures, twisted pair, #22-gauge, 100- Ω lines are used. The drivers are 7438 open collector, high current TTL-buffer, 2-input NAND-gates, and the receivers are regular 7400 NAND inputs. Both ends of the lines are terminated with 150 Ω to +5V and 330 Ω to ground. The common term is terminated on the GND pin of the driver and receiver chip, respectively.

III. Signal Sync and Noise Filter

In order to combat noise and to synchronize the interface timing control signals with the internal service clock of the computer, a signal transition is recognized only upon the second consecutive sample of the internal clock. This specification is valid for transitions in either direction. Stated differently, a single noise pulse of either polarity of a duration of less than two clock periods occurring at any time will have no effect on the true operation of the line receiving logic.

IV. Timing Control Line Operation

Figure 1 shows the selected set of computer interface timing control lines together with eight data lines. The request-to-transmit line is unidirectional, while the return response and data lines are half-duplex bidirectional. For bidirectional communication, two request-to-transmit lines are then required, one in each direction, as shown. Figure 5 is a simple block diagram and timing chart which shows the detailed operation of the timing control lines. The time sequence for the various control lines, which is repeated for each linear bit or parallel byte, is listed as follows:

- (1) An outbound request line is asserted by the transmitting device.
- (2) The assertion of an inbound request line is sampled and synchronized by the recipient device.
- (3) The synchronized inbound request signal causes assertion of the outbound return response line.
- (4) The return response line inbound to the transmitting device is sampled and synchronized and causes assertion of the outbound ready line.
- (5) The ready signal inbound to the recipient device is sampled and synchronized, and used to form a data-strobe pulse for sampling the received data.
- (6) Upon sampling the received data, the inbound ready signal is used to turn off the outbound response line.

- (7) Turnoff of the outbound response line will in turn cause turnoff of the inbound ready line.
- (8) Turnoff of the inbound ready line will again cause the outbound response line to turn on, conditional on the request line being on, for receiving of the next character.
- (9) At the end of a block transmission, the request line is turned off by the transmitting device simultaneously with the ready line, outbound from the transmitting device, for the last character being turned on.

A. Control Logic Operation

The operation of a signal synchronizing and noise control receiving register for the transmission interface timing control signals, in general, and for the ready line register, in particular, is specified as follows:

- (1) A signal change is recognized only if the signal remains in its new state for two consecutive clock periods after the signal has remained in its prior state for at least two clock periods.
- (2) A data strobe will be generated only for a unidirectional change of the input signal.
- (3) Once a data-strobe pulse has begun to form, it will be completed independently, and the fact that it was completed will be independently reported. Independently, as used here, implies independence of what is happening on the input signal line.
- (4) A noise spike of either polarity of a duration less than two clock periods occurring at any time must not be the cause of a double data-strobe pulse, nor should such a noise spike interrupt the forming of a data-strobe pulse or the subsequent report signal that a data-strobe pulse was formed.

B. Request Line Sync Register

Figure 6 shows the interface timing control logic. The logic is implemented with a SN5495 universal 4-bit, shift-right, parallel-load register with no additional gating. The input signal is used as a mode control and the parallel entries are connected so that the register, when it is in the parallel load mode, will shift left. The shift-right/shift-left data entries are fixed-wired as "1" and "0," respectively. The desired output level is achieved by correlating the input mode control signal with the fixed-wired data inputs; e.g., SR = 1, SL = 0, or vice versa.

The output of stage C will change state only if the output line has been stable for two consecutive clock pulses, as described. This is true for transitions in either direction, and it is true in general. There are however, two special cases in which it is not true, and that is if the line reverses again between the first and second or the second and third clock pulses following a transition. The probability of this special case occurring is deemed exceedingly low. The output from stage B is used directly as the response term, conditional only on a ready register term. The reason that the direct connection is acceptable, as opposed to the use of an intermediate storage device, is that when the request line is turned off at the same time that the ready line is turned on, for one character transfer or for the last character in a block, the turnoff of the response line, which in turn causes the ready line to turn off, occurs at the same time that the data-strobe pulse begins to develop. The request line register and the ready line register are connected in much the same manner. Furthermore, if the same type of interface logic is used at both the transmitting and receiving ends, there is the added sync delay at the transmitting end between its inbound response line turnoff and the time that its outbound ready line is turned off. Stated differently, the request line turns off the response line, which in turn turns off the ready line. Whether it is for a single character transfer, or for the last character, the response line is turned off sooner than for a character within a block, where it is turned off at the end of the data-strobe pulse. The ready line is still turned off one clock period later than completion of the data-strobe pulse.

C. Ready Line Sync Register

As shown in Fig. 6, the ready register is connected to shift right in either of its modes. The parallel load entries are connected to shift right; however, with certain modifications. The input signal is used as mode control; the data entry for shift right in the serial mode is a fixed 0 and for shift right in the parallel-load mode a fixed 1. By shifting in one direction only, the vector that generates the data strobe is automatically generated for a unidirectional signal change only. The external gating shown in Fig. 2 is intended primarily to prevent one-clock-period noise pulses from generating or regenerating the strobe pulse, or to interfere with its forming, or with the reporting of its having been formed.

As shown in the truth table (Fig. 7), the strobe pulse condition is ABC and the strobe pulse completion report

condition is BC, both of which can occur only for the specified conditions. In relation to the truth table, the ready register connection shown in Fig. 2 is derived from the following arguments: When the input signal is a 1, a 1 is entered to the shift-right connected entry of the register. When the signal is a 0, a "0" is entered to the serial input of the internally connected shift-right register. The content in B is always entered to C, while the entry to B is a function of the signal and the content of the register. The signal is the mode-control term, and when it is 0, the shift register is internally connected for shift right. What is in A will, in this mode, always be shifted to B. When the signal is a 1, a "1" is entered to the input of the shift register, which in this mode is connected externally to shift right to allow for vector modification. Thus, in this mode, what is in A is shifted into B in all instances except one: the 011 condition, in which case, a 1 is entered to B instead of the 0 in A.

D. Response-Ready Register Time Share

The response and ready lines are both bidirectional but are always energized from opposite ends; the request line is always energized first and the response line second. This allows time-sharing a single synchronizing receiving register between these two lines, as shown in Fig. 8. (Figures 1, 5, 6, 7 and 8, are taken from JPL Specification ES508535 A, Appendix, a JPL internal document.) Also shown in the figure are the steering gates for time-sharing of the ready-response register through the synchronized request line. The same line is also used for added interlock of the outbound response line and the outbound ready line.

The control logic described here is duplicated in each end of a transmission path.

V. Data Transfer Rates

The bit transfer rate for different length cables has been tabulated using the type of interface described here, where the assertion and/or release of a line is recognized only on the second clock pulse of an internal 5-MHz service clock, and using identical interface logic at both ends, with individual service clocks (Table 1).

A cable delay of 5.90 ns/m is used, and a double round-trip per byte for continuous transmission is considered. The cable length has been limited to 152.4 m so that the signal attenuation will not cause a marginal operation.

Table 1. NCS standard computer interface transfer rates for various cable lengths ^a

Cable length, m	Maximum reliable data transfer rate in kilobytes/s
3.05	530
15.24	460
30.48	400
60.96	310
152.4	185

^aAsynchronous internal service clocks of 5 MHz at each end.

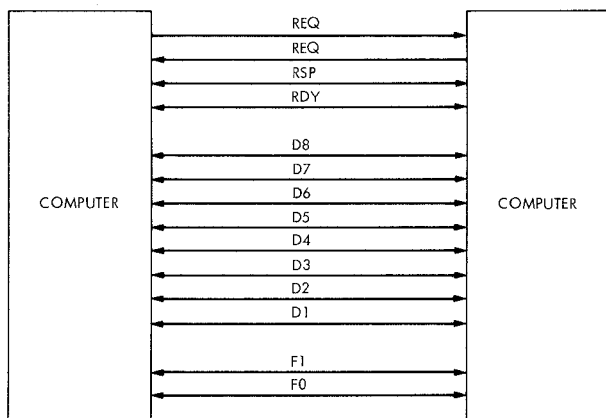


Fig. 1. NCS standard computer interface hardware lines

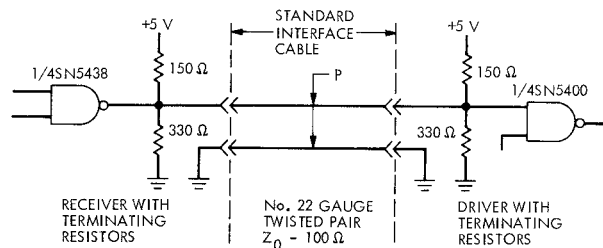


Fig. 2. NCS standard computer interface unidirectional line driver/receiver configuration

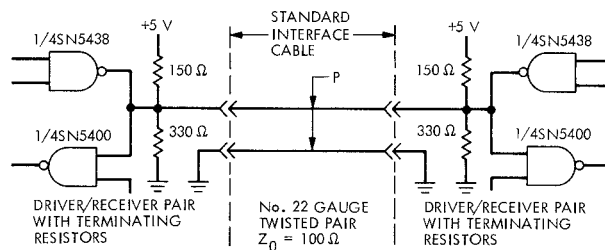


Fig. 3. NCS standard computer interface bidirectional line driver/receiver configuration

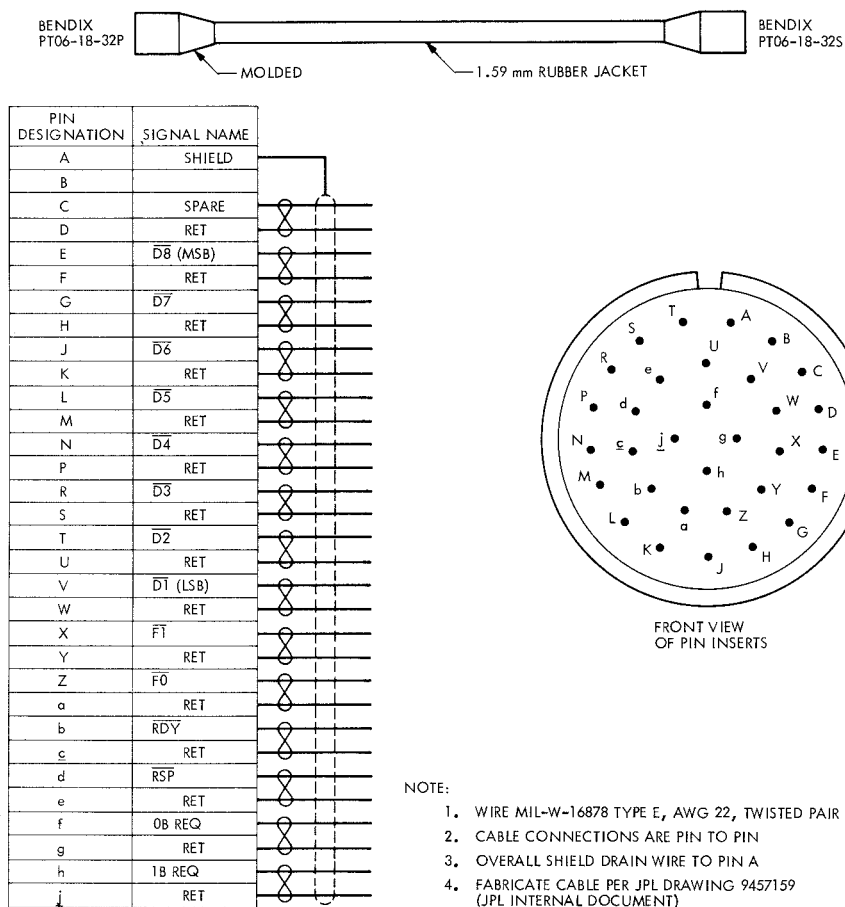


Fig. 4. NCS standard computer interface cable connector and pin assignment

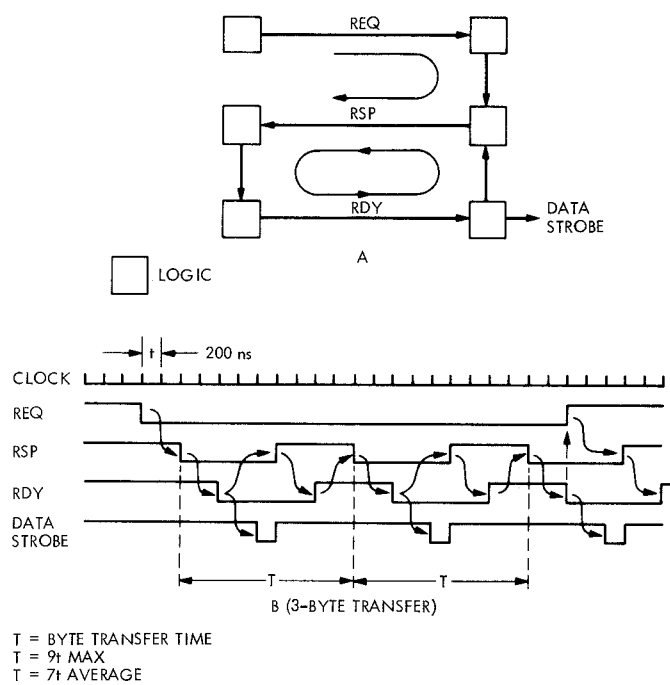


Fig. 5. NCS standard computer interface timing control line, logic, and timing diagram

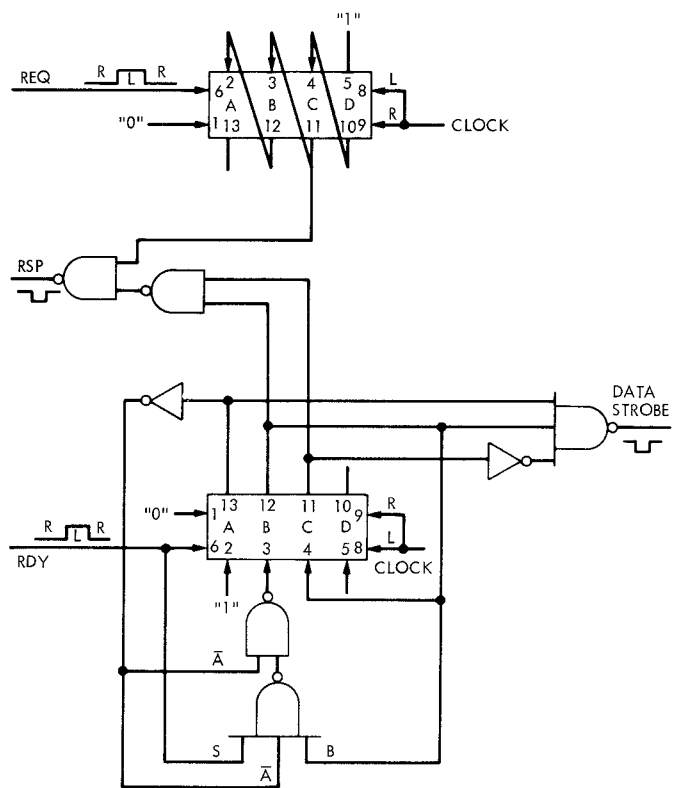


Fig. 6. NCS standard computer interface, basic interface timing control logic

S	A	B	C	S	A	B	C
0	0	0	0	1	1	1	1
1	0	0	0	0	1	1	1
1	1	0	0	0	0	1	1
0	1	1	0	1	0	0	1
0	0	1	1	1	1	0	0
1	0	0	1	0	1	1	0
1	1	0	0	0	0	1	1
0	1	1	0	1	0	0	1
0	0	1	1	1	1	0	0
0	0	0	1	1	1	1	0
0	0	0	0	1	1	1	1
0	0	0	0	1	1	1	1
1	0	0	0	0	1	1	1
0	1	0	0	1	0	1	1
1	0	1	0	0	1	1	1
0	1	0	1	1	0	1	1
1	0	1	0	0	1	1	1
0	1	0	1	1	0	1	1
0	0	1	0	1	1	1	1
1	0	1	0	0	1	0	1
1	1	0	1	0	0	1	0
1	1	1	0	0	0	0	1
1	1	1	1	0	0	0	0
1	1	1	1	0	0	0	0

Fig. 7. (contd)

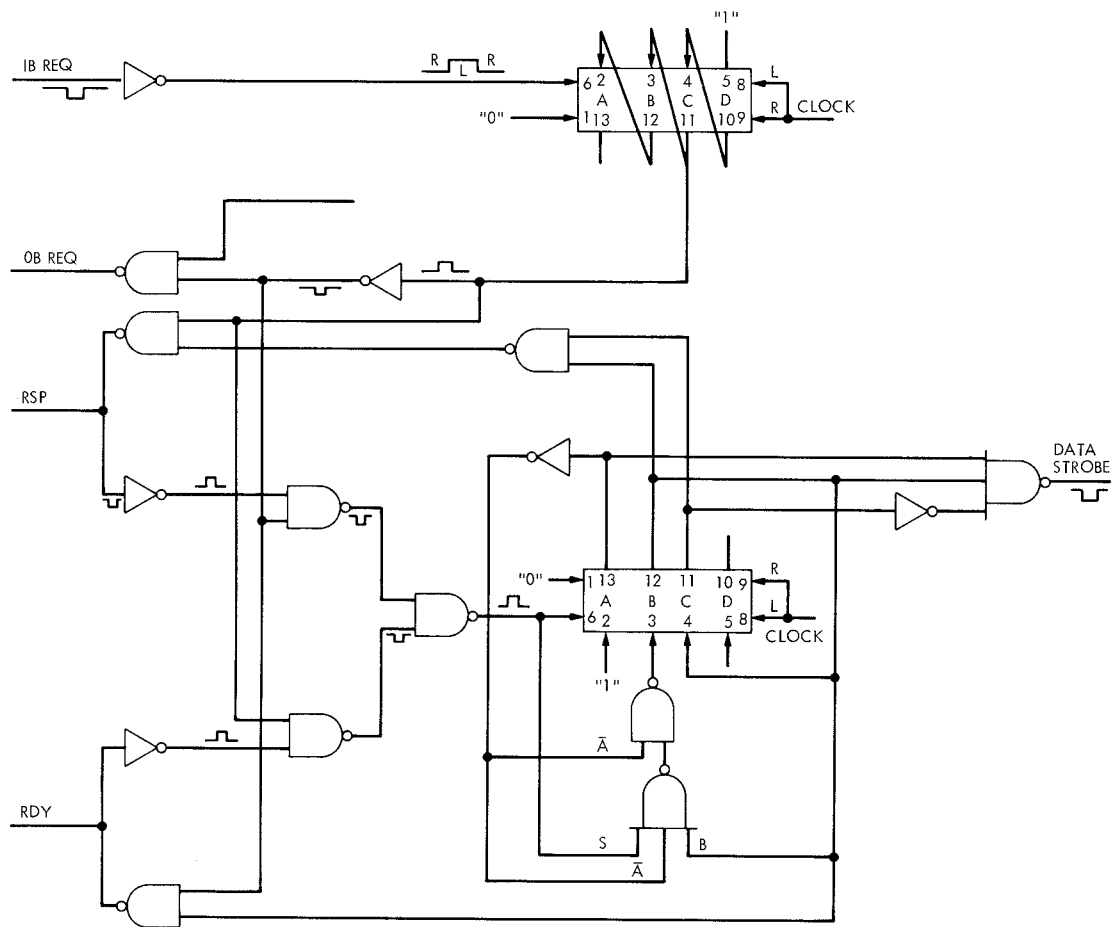


Fig. 8. NCS standard computer interface timing control logic including interlock and time share